SUBSTITUTE SPECIFICATION

GATED CLOCK RECOVERY CIRCUIT

Field of the Invention

The present invention relates to clock recovery circuits, and more particularly, to circuits that operate in a burst mode to recover the clock signal from an early bit in the incoming data.

Background of the Invention

In a communication system, the transmitter has clock circuitry that controls the speed at which data is transferred via a communications medium. The receiver also has clock circuitry that controls the speed at which the data that is received from the communications medium is processed. Ideally, the receiver's clock and the transmitter's clock will operate at exactly the same frequency and will be appropriately aligned in phase. The transmitter's clock and the receiver's clock, however, are typically close but not identical in frequency, resulting in frequency mismatch.

Receivers in many digital communication systems recover the clock signal directly from the incoming data sequence, typically using a phase-locked loop (PLL) circuit. In such an implementation, the PLL circuits generate a local clock signal that is phase aligned with the incoming reference signal. The phase aligned local clock signal facilitates the receipt and processing of synchronous data sent by a transmitter in the communication system.

Typically, conventional PLL circuits include a phase detector, a filter and a voltage-controlled oscillator (VCO). In the conventional PLL circuit, the phase detector compares the incoming reference signal (DATA) and the output of the VCO. The phase detector generates an error signal that is representative of the phase difference of the reference signal and the VCO output. The error signal is filtered and applied to the control input of the VCO to produce an output signal that tracks the phase of the reference signal.

Many clock recovery circuits operate in a continuous mode, where the transmitter and receiver continuously operate and monitor communication ports for arriving data. Such continuous operation, however, requires a significant amount of power, which is particularly

problematic for battery-powered receivers, such as those deployed in wireless or optical communication systems. Thus, it is desirable to conserve power in such receivers by operating only when there is data to be processed. Thus, a number of clock recovery circuits have been proposed or suggested that operate in a burst mode to quickly adjust to phase changes in data coming from the communications medium. See, for example, U.S. Pat. No. 5,757,872, entitled "Clock Recovery Circuit," assigned to the assignee of the present invention, and incorporated by reference herein.

In addition to providing improved power consumption characteristics, such burst mode clock recovery circuits also do not require a long string of binary transitions to generate a clock signal that has the same frequency and appropriate phase alignment with the incoming data. While such burst mode clock recovery circuits exhibit improved performance relative to continuous mode clock recovery circuits, they suffer from a number of limitations, which, if overcome, could expand the utility and efficiency of burst mode clock recovery circuits. For example, most burst mode clock recovery circuits exhibit mismatch between the oscillators, thereby causing a frequency offset. A need therefore exists for a method and apparatus for recovering a clock signal from an incoming reference signal that has matched oscillators without a frequency offset.

Summary of the Invention

A gated clock recovery circuit is disclosed that receives an input data stream and generates a frequency and phase aligned clock output. The gated clock recovery circuit substantially instantaneously adjusts the generated clock output to phase changes in the incoming data stream. In addition, the gated clock recovery circuit generates the clock output signal using only transmitted non-predetermined data. In other words, the gated clock recovery circuit of the present invention can generate a clock signal having a frequency and phase that are substantially aligned with the clock of the transmitter, without requiring any specific transition pattern or consecutive string of binary "1s" or "0s."

According to one aspect of the invention, the gated clock recovery circuit includes two PLL circuits. The first PLL (PLL1) initially adjusts to the frequency of a local clock reference and indirectly tunes the second PLL (PLL2). In this manner, the second PLL

immediately adjusts to the phase of the received data, once such incoming data is received and maintains this phase relationship between the second oscillator and the received data.

Brief Description of the Drawings

FIG. 1 is a schematic block diagram illustrating a communication system in which the present invention may be used;

FIG. 2 is a schematic block diagram illustrating the receiver of FIG. 1 in further detail; and

FIG. 3 is a schematic block diagram illustrating the clock recovery circuit of FIG. 2 in further detail, in accordance with the present invention.

Detailed Description

FIG. 1 illustrates a communication system 100 in accordance with the present invention. As shown in FIG. 1, the communication system 100 is comprised of a transmitter 102, a communications medium 104, and a receiver 200, discussed further below in conjunction with FIG. 2, connected as shown. Data 108 is output by the transmitter 102, carried by the communications medium 104, and arrives at the receiver 200 as an input data stream 107. The receiver 200 decodes the data signal to produce an output data stream 110.

FIG. 2 shows the receiver 200 of FIG. 1 in further detail. As shown in FIG. 2, the receiver 200 includes a preprocessing circuit 202 that processes the input data stream 107 to produce a data signal 204. The data signal 204 is input into a clock recovery circuit 300, discussed further below in conjunction with FIG. 3, in accordance with the present invention. The clock recovery circuit 300 uses the data signal 204 to generate a clock signal 208 having a proper phase relationship with the data signal 204. An optional elastic storage circuit 210 can be included for jitter reduction. The elastic storage circuit 210 may be embodied, for example, using the elastic storage circuits, such as (i) a demultiplexer; or (ii) a set of memory storage elements and a set of logic elements interconnected to operate as a first-in-first-out circuit, described in U.S. Pat. No. 5,757,872, entitled " Clock Recovery Circuit," assigned to the assignee of the present invention, and incorporated by reference herein.

The optional elastic storage circuit 210 has a first input 209 that receives the clock signal 208 and has an output 211 that outputs the output data stream 110. The elastic storage circuit 210 has a second input 212 and a third input 213. The second input 212 accepts the data signal 204 representing the input data stream 107. In this embodiment, the data signal 204 is input directly into the second input. As will be apparent to those skilled in the art, flip-flops may be used to provide delay and/or synchronization such that the clock signal 208 and the data signal 204 are in proper relationship. The third input 213 accepts a local clock signal 214.

FIG. 3 is a schematic block diagram illustrating the clock recovery circuit 300 of FIG. 2 in further detail. As shown in FIG. 3, the clock recovery circuit 300 includes two PLL circuits 310 and 350. According to one feature of the present invention, the clock recovery circuit 300 can generate a clock signal having the same frequency and appropriate phase alignment with the incoming data 328, without requiring any specific transition pattern or strings of binary "1" or "0." As discussed hereinafter, the first PLL 310 initially adjusts to the frequency of the transmitter and indirectly tunes the second PLL 350. In this manner, the second PLL 350 can immediately adjust to the phase of the transmitter, once incoming data is received.

More specifically, the first PLL 310 adjusts to the frequency of the incoming data, and provides a bias voltage, CAP1, to the second PLL 350 to indirectly initially tune the second PLL 350. The bias voltage, CAP1, 325 is applied to the second PLL 350 through a two-position transmission gate (or switch) 340 (short or open) that is initially in a closed (short) position, until a reset signal is received on the DRESET line 327. The transmission gate (or switch) 340 may be embodied as any device that imposes the bias (or current) of the first PLL 310 onto the second PLL 350. In one embodiment, the transmission gate 340 is placed in an open position once data is detected on the DATA line 328. Thus, the first PLL 310 drives the bias voltage, CAP2, of the second PLL 350, to align the frequency with the incoming data, until received data opens the transmission gate 340. Thereafter, the bias voltage, CAP1, is removed and the second PLL 350 can operate without being controlled by PLL1 310. Thereafter, the second PLL 350 oscillates in phase with the received data.

As shown in FIG. 3, the first PLL 310 includes a frequency detector 312, a filter 314 and an oscillator 318, such as a voltage-controlled oscillator. The frequency detector 312 compares the phase of the local reference signal (CLOCK) and the output (PHACLK) of the

oscillator 318. It is noted that the local reference signal (CLOCK) operates at the same nominal frequency of the transmitter. Thus, the frequency detector 312 generates an error signal (FDETOUT1) representing the phase difference of the reference signal and the oscillator output. The error signal is filtered by the filter 314 and the bias signals (BIASP1 and BIASN1) serve to adjust the frequency of the oscillator 318 in an upward or downward manner, respectively, and the bias signals (BIASP1 and BIASN1) are integrated over time to correspondingly adjust the phase of the oscillator output. The bias signals (BIASP1 and BIASN1) are applied to the corresponding control inputs of the oscillator to produce an output signal (PHACLK) that tracks the phase of the reference signal. It is noted that while the illustrative embodiment employs two bias signals (BIASP1 and BIASN1), one or more could be employed, as would be apparent to a person of ordinary skill in the art.

Likewise, as shown in FIG. 3, the second PLL 350 includes a phase detector 400, a filter 354 and an oscillator 358, such as a voltage-controlled oscillator (VCO). The phase detector 400 compares the phase of the incoming reference signal (DATA), as appropriately delayed by the matching data delay stage 360, and the output (OSC) of the oscillator 358. It is noted that the matching data delay stage 360 introduces the same delay to the incoming reference signal (DATA) as the delay introduced by the RUNGEN 305, discussed below, and the oscillator 358. The PHASEDET 400 generates an error signal (FDETOUT2) representing the phase difference of the reference signal IDATDEL and the oscillator output (OSC). The error signal is filtered by the filter 354 and the bias signals (BIASP2 and BIASN2) are applied to the corresponding control inputs of the oscillator to produce an output signal (OSC) that tracks the phase of the reference signal. It is again noted that when the transmission gate 340 is in a closed (short) position, the second PLL 350 is controlled by the bias signal (CAP1) produced by the first PLL 310, VCO 358 is turned off, and FDETOUT2 gives no error signal.

The first PLL 310 should be generally designed with substantially matching characteristics to the second PLL 350. Thus, the oscillators OSC1 and OSC2 318, 358 and the voltage on the capacitors CAP1 and CAP2 in the filters 314 and 354 should be matched. The first-in-first-out (FIFO) 380 is an implementation of the elastic storage circuit 210, discussed above, for jitter reduction. It is noted, however, that the first PLL 310 and the second PLL 350 can be designed with differences in frequency, for example, to allow an offset with a clock

signal. For example, the PLLs 310, 350 can be embodied as ring oscillators, each having an odd, but unequal, number of invertors. In such an embodiment, the voltage on the capacitors CAP1 and CAP2 in the filters 314 and 354 can still be matched. For example, if the desired clock operates at 50 MHz, the circuit 300 can operate at 500 MHZ when PLL1 310 has a delay line that is ten times longer than PLL2 350.

RUNGEN 305 is control circuitry that receives DATA 328 and DRESET 327. The output, IRUNDEL, connects the two sides of the transmission gate 340 and stops OSC2 358 upon receiving a DRESET 327. After the DRESET signal 327 goes away, the next received data causes IRUNDEL to open the transmission gate 340 and start OSC2 358 in phase with IDATDEL.

It is to be understood that the embodiments and variations shown and described herein are merely illustrative of the principles of this invention and that various modifications may be implemented by those skilled in the art without departing from the scope and spirit of the invention.